

AD3100

Audio Synchronizers

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STANDARD EQUIPMENT WARRANTY

Pixel warrants that the goods sold under this contract will be free from defects in material and workmanship for a period of one year from purchase, and this warranty will be limited to the repair and/or replacement of parts and the necessary labor and services required to repair the goods in our location.

Customer will be responsible for shipping the unit to Pixel freight and Pixel will repair or replace the unit at its option and return to the customer via prepaid freight.

IT IS EXPRESSLY AGREED THAT THIS WARRANTY WILL BE IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING THE WARRANTIES OF FITNESS AND MERCHANTABILITY.

SAFETY SUMMARY

The general safety information in this part to summary is for both operating in series in personnel.

Power Source

This product is intended to operate from a power module connected to a power source that do not apply more than 125 V RMS (or 250 V when unit is wired to operate from 220V or 240V supplies) between the supply conductors or between either, supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Ground the Product

This product is grounded through the grounding conductor of the power module of power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power module cord is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Use the Proper Fuse

To avoid fire hazard, use only the fuse of correct type (Pixel products use slow-blow fuses), voltage rating, and current rating as specified in the parts list for your product. Refer fuse replacement to qualified service personnel.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere.

To Not Operate Without Covers

To avoid the personal injury, do not remove product covers or panels. To not operate the product without the covers and panels properly installed.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid in resuscitation is present. When performing a service use isolation transformer to provide power. Replace parts with the same voltage ratings, and current ratings as specified in the parts list for your product. And current

Introduction

The AD3100 digital audio processor is ideally suited for a wide range of audio applications in production and post-production. With both, analog and digital inputs the AD3100 is well suited for analog, digital and hybrid installations. The AD3100 can be used as a variable pitch shifter; time compressor / expander; automatic lip sink corrector; variable audio delay up to 6.144 seconds; sample rate converter for digital audio and as a trans-coder between analog and digital audio formats.

Pitch shift is manually adjustable from 0 to $\pm 25.0\%$ in 0.1% increments. This function can be applied to counteract pitch error which may be present on incoming audio.

Delay is manually or automatically adjustable from 0 to 6.144 seconds with 1 millisecond resolution. The maximum rate of delay change is manually adjustable from 0.2% to 10% in 0.1% increments. Internal pitch shifting is automatically applied when necessary during delay change, to counteract the undesired pitch modification which would otherwise occur. Thus, rapid delay changes are possible. The unit may also be operated so as to cascade pitch shift with a fixed audio delay.

A time compression/expansion **-TIMEMAKER™** - mode allows the duration of a segment of program material to be decreased or increased, while retaining the original pitch.

A dump mode is available, which produces instantaneous zero delay, for obscenity screening.

A flexible digital audio interface is also provided, which supports AES/EBU, SMPTE, or S/PDIF format. Any sample rate between 25 and 48 kHz may be received. Input sample rate conversion circuitry converts the incoming rate to an internal, crystal oscillator derived, 48 kHz sample rate. Attenuation of incoming sample clock jitter is inherent in this input rate conversion process.

Delay and pitch digital signal processing, analog-to-digital conversion, and digital-to-analog conversion all take place at the crystal oscillator derived 48 kHz internal sample rate.

Output sample rate conversion circuitry produces digital audio output, available at a selectable rate of 48, 44.1, 44.056, or 32 kHz. Thus, sample rate conversion between the digital audio interface input and output may be performed. Alternatively, analog audio may be converted to digital audio at 48, 44.1, 44.056, or 32 kHz. Any of these four output sample rates may be frequency locked to an input sample rate of 48, 44.1, 44.056, or 32 kHz, in any combination. Any of these four of the sample rates may alternatively be frequency locked to externally supplied NTSC or PAL video, or to an internal crystal oscillator reference.

While the input source may be selected as either analog or digital audio, both analog and digital audio outputs are always simultaneously available.

Control inputs may be entered via a front-panel keypad. A front panel liquid crystal display shows delay and pitch shift. LED-s display digital audio sample rate and status indication. An LED bar graph meter displays stereo audio input signal level.

A rear panel RS-232 port supports remote control and status monitoring.

The unit can accept delay steering inputs from the Pixel DD-2100 Video Delay Detector.

A block diagram depicting audio and control signal flow is included in Theory of operation section.

Technical specifications

Pitch Correction

Adjustable from 0 to $\pm 25\%$ in 0.1% increments

Delay Setting

Adjustable from 0 to 6.144 sec in 1 ms increments

Rate of Delay Change

Adjustable from 0.2% to 10% in 0.1% increments

ANALOG INPUT AND A-TO-D CONVERSION

Input Configuration:	Balanced
Input Impedance:	20 k Ω or 600 Ω , selectable
Full Scale Input Level:	+28, +24, or +20 dBu, selectable
Maximum Input Level:	+28 dBu
Gain Trim:	0 to -20 dB
Encoding Format:	20 bit linear PCM, 48 kHz sample rate, delta-sigma modulation, 64X over-sampling.

D-TO-A CONVERSION AND ANALOG OUTPUT

Output Configuration:	Balanced
Output Impedance:	24 Ω maximum
Full Scale Output Level:	+28, +24, or +20 dBu, into 600 Ω , selectable
Gain Trim:	0 to -20 dB
Encoding Format:	20 bit linear PCM, 48 kHz sample rate, 8X over-sampling

DIGITAL AUDIO INTERFACE

Types:	AES/EBU, SMPTE, S/PDIF
Sample Rates:	48 kHz, 44.1 kHz, 44.056 kHz, 32 kHz. Output rate may be independent of input rate.
Connectors:	XLR (AES/EBU), BNC (SMPTE), RCA (S/PDIF)
Impedance:	110 Ω balanced (AES/EBU), 75 Ω unbalanced (SMPTE and S/PDIF)
Internal Reference	
Frequency Stability:	± 25 ppm maximum
Video Reference	
Horizontal Frequencies:	15734.26 Hz (NTSC), or 15625 Hz (PAL)

**Video Ref. Frequency
Capture + Lock Range:** ± 50 ppm minimum

AUDIO PERFORMANCE, ANALOG INPUT TO ANALOG OUTPUT

Frequency Response: ± 0.1 dB maximum from 20 Hz to 20 kHz
Dynamic Range: 97 dB minimum, 20 Hz - 20 kHz, un-weighted
THD+N: .005% maximum, 20 Hz - 20 kHz, un-weighted, @ +23 dBu
SMPTE IM: .015% maximum @ +23 dBu
Channel Separation: >80 dB, 20 Hz - 20 kHz
Channel Phase Match: ± 1 degree maximum, 20 Hz - 20 kHz
Transport Delay: 1.5 ms maximum

(All measurements made with +24 dBu full scale input/output levels selected, fixed audio delay, zero pitch shift)

AUDIO PERFORMANCE, DIGITAL AUDIO INPUT TO DIGITAL AUDIO OUTPUT

Frequency Response: ± .01 dB maximum from 20 Hz to 20 kHz
Dynamic Range: 117 dB minimum, 20 Hz - 20 kHz, un-weighted
THD+N: .003% maximum, 20 Hz - 20 kHz, un-weighted, @ -1 dBFS
SMPTE IM: .005% maximum, @ -1 dBFS
Channel Phase Match: 0 degrees maximum
Transport Delay: 2.3 ms maximum

(All measurements made with 48 kHz sample rate, fixed audio delay, zero pitch shift)

CONTROL

Serial Remote: 4 pin telephone handset jack, accepts steering input from DD- 2100
Remote Dump: 1/4" stereo phone jack, closure to ground on tip activates dump mode.
Delay Pulse Input: BNC connector accepts active-high TTL pulse steering input.
RS-232 Port: DE-9 connector provides two-way communication.

FRONT PANEL DISPLAYS

Input Level: Dual LED bar graph
Status and modes: 20 X 2 LCD plus LED indicators

POWER

AC Input: 110-120/220-240 VAC, 50/60 Hz, TBD Watts maximum

ENVIRONMENTAL

Operating Temperature:	0°C to 45°C
Storage Temperature:	-25°C to +75°C
Humidity:	10% - 95%, non-condensing

MECHANICAL

Width:	19.0" (48.3 cm)
Height:	1.75" (4.5 cm)
Depth:	19.5" (49.5 cm) overall
Weight:	9.8 lb (4.5 kg)

Note: Specifications subject to change without notice.

Setup

Please refer to the "AD3100/TC3100 AUDIO INPUT/OUTPUT CONFIGURATION CHART". This chart, and accompanying footnotes, summarizes connections, certain PC Board Jumper positions, and setup menu selections for 16 combinations of input and output formats. Information relevant to signal characteristics is also provided.

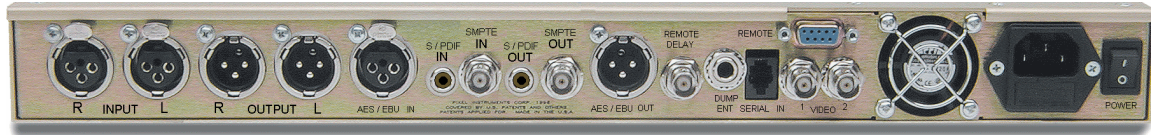
Jumper and switch positions should be established prior to operation. The following descriptions provide information additional to that found on the configuration chart. The jumpers and switches described immediately below are located on the PC board, and are highlighted on the "JUMPER AND SWITCH CONFIGURATION CHART".

1. E1 and E2: Select the digital audio input connector. For AES/EBU operation, E1 and E2 must be in the "AES/EBU" position. In this position, the S/PDIF IN and SMPTE IN connectors will be inoperative. For S/PDIF or SMPTE operation, E1 and E2 must be placed in the "SPDIF/SMPTE" position. In this position, the AES/EBU IN connector will be inoperative.
2. E3 and E4: Select the 75 Ω unbalanced digital audio output level. In the "SPDIF" position, nominal output level is 0.5V pk-pk. In the "SMPTE" position, nominal output level is 1 V pk-pk.
3. JP11: Connects shield of cable attached to the AES/EBU IN connector to AD3100 signal ground (which also connects to chassis ground). Factory default is jumper installed.
4. S3, S5: Select termination of analog L INPUT and R INPUT, respectively. A termination of 600 Ω is selected by the "600" position. In the other position, a termination of 20 k Ω is selected. The 600 Ω position is the factory default.
5. S4, S6: Two position DIP switches, used to select one of three nominal full-scale analog levels for the L INPUT and R INPUT, respectively. +28 dBu full-scale is selected when both positions are "Open". +24 dBu full-scale is selected when Position 1 is "Open", and Position 2 is "Closed". +20 dBu full-scale is selected when both positions are "Closed".
6. S7, S8: Two position DIP switches, which are used to select one of three nominal full-scale analog output levels at the L OUTPUT and R OUTPUT, respectively. +28 dBu full-scale is selected when both positions are "Closed". +24 dBu full-scale is selected when Position 1 is "Closed", and Position 2 is "Open". +20 dBu is selected when both positions are "Open".

The positions of jumpers and switches which appear on the PC board but which are not described above do not require modification for normal operation. The functions of these other jumpers and switches are documented in Appendix C.

Rear Panel Connectors

This section describes the rear panel signal connectors and functions.



1. R INPUT and L INPUT: Three-pin female XLR connectors, which provide for the application of balanced analog audio inputs. Phasing is such that Pins 2 and 3 correspond to non-inverting and inverting inputs, respectively, with regard to digital audio sample word polarity. The input level applied to the R INPUT and L INPUT must not exceed +28 dBu.
2. R OUTPUT and L OUTPUT: Three-pin male XLR connectors, which output balanced analog audio. Phasing is such that Pins 2 and 3 correspond to non-inverting and inverting outputs, respectively, with regard to digital audio sample word polarity. The load impedance applied to R OUTPUT or L OUTPUT should be not less than 600 Ω . of the red-hot to happen
3. AES/EBU IN: A three-pin XLR female connector, which provides for the application of a 110 Ω balanced AES/EBU digital audio signal. Pin 1, the cable shield connection, may be optionally disconnected from the AD3100 signal ground and chassis ground by removing JP11 (see "SETUP" section).
4. S/PDIF IN: An RCA female connector, which provides for the application of 75 Ω unbalanced S/PDIF digital audio signal. The connector shell is attached to the AD3100 signal ground (which also connects to chassis ground).
5. SMPTE IN: A BNC female connector, which provides for the application of a 75 Ω unbalanced SMPTE digital audio signal. The connector shell is attached to the AD3100 signal/chassis ground. SMPTE IN is connected in parallel with S/PDIF IN. Thus, signals should not be applied to both simultaneously.
6. S/PDIF OUT: An RCA female connector, which outputs 75 Ω unbalanced S/PDIF digital audio. S/PDIF out is transformer-driven, and both the center contact and shell are isolated from the AD3100 signal ground and chassis ground.
7. SMPTE OUT: A BNC female connector, which outputs 75 Ω unbalanced SMPTE digital audio. SMPTE OUT is connected in parallel with S/PDIF OUT. Thus, SMPTE OUT center contact and shell are also isolated from the AD3100 signal ground and chassis ground.
8. AES/EBU OUT: A three-pin XLR male connector, which outputs 110 Ω balanced AES/EBU digital audio. Pin 1 connects to the AD3100 signal/chassis ground.
9. REMOTE DELAY: A BNC female connector, which provides for a delay-steering input in the form of an active-high TTL pulse. The high period corresponds to the delay quantity. Such a signal is available from the Pixel DD-2100 Video Delay Detector DDO PULSE OUT connector. REMOTE DELAY terminates in 75 Ω .

10. DUMP/ENTER: A stereo 1/4" phone jack, which provides for contact-closure activation of the dump mode. Dump mode is activated when continuity is established between the tip and shield.

11. SERIAL IN: A 4-pin modular handset connector, which provides for the application of a serial digital delay steering input. Such a signal is available from the Pixel DD-2100 SERIAL OUT connector. Signals should not be simultaneously applied to the SERIAL IN and REMOTE DELAY connectors.

12. VIDEO 1 and VIDEO 2: Two BNC female connectors, which provide for the application of NTSC or PAL base-band video as a digital audio output frequency reference. VIDEO 1 and VIDEO 2 are connected for high-impedance loop-through. External 75 Ω termination should be provided.

13. REMOTE: A DE-9 female connector is RS-232 interface which can be used for control and status monitoring via external Pixel RC-3100 Remote. Information on RC-3100 is contained in the manual for that product.

If power is removed from the AD3100, or if an internal DC power supply voltage out-of-tolerance condition is detected, internal bypass relays drop out. When this occurs, L INPUT is connected to L OUTPUT, R INPUT is connected to R OUTPUT, AES/EBU IN is connected to AES/EBU OUT, and S/PDIF and SMPTE IN are connected to S/PDIF and SMPTE OUT. Under bypass conditions, the S/PDIF OUT and SMPTE OUT shells are connected by relay contacts to AD3100 signal/chassis ground.

Front Panel Displays and Indicators



1. Liquid Crystal Display (LCD): A backlit 2-line by 20 character panel displays pitch shift and current delay. Additionally, control and setup menus, setup status, help messages, and keypad inputs are displayed.

2. SAMPLE RATE IN LED's: If the digital audio input sample rate is within ± 400 ppm of 32, 44.056, 44.1, or 48 kHz, as measured against the AD3100 internal frequency reference, the corresponding LED illuminates. If some other sample rate is present, or no digital audio signal is present, all SAMPLE RATE IN LED's are blanked.

3. SAMPLE RATE OUT LED's: The LED corresponding to digital audio output sample rate illuminates.

4. INPUT LED: This indicator is a summary alarm for the digital audio input. It encompasses confidence, lock, code, parity, and validity errors. A confidence error occurs when the received data eye opening is less than half a bit period, and indicates a physical data link which is marginal and does not meet specifications of applicable standards documents. A lock error occurs when

the receiver PLL is not locked. A code error occurs when a bi-phase coding error is detected. The digital audio sub-frame format contains a validity bit, which is set to zero by the transmitter to indicate the associated sample is suitable for conversion to audio. A validity error occurs if the received validity bit is a "1".

INPUT illuminates green if none of the above listed errors is detected, and Input Source Digital function (see OPERATION section) is selected. INPUT illuminates red if one or more error is detected. Confidence or validity errors may be considered "soft" errors, which do not necessarily mean that an audio sample error has occurred. The received validity bit is passed through unchanged and is re-transmitted with the digital audio output.

If the Input Source Analog function (see OPERATION section) is selected, INPUT does not apply, and is extinguished. In this case, the transmitted validity bit is "0".

5. IN LOCK LED: Illuminates green if the digital audio receiver PLL is locked; illuminates red otherwise. The red condition typically indicates an input signal which is missing, or a sample rate outside the receiver lock range. The IN LOCK LED is enabled whenever the INPUT SOURCE DIGITAL function is selected. The IN LOCK LED is also enabled if the INPUT SOURCE ANALOG and OUTPUT FREQUENCY REF - DIGITAL INPUT (see OPERATION section) functions are selected. Otherwise, the IN LOCK LED is extinguished.

6. OUT LOCK LED: Illuminates green if the digital audio output sample rate synthesizer PLL is locked, red otherwise. A red indication typically results if the OUTPUT FREQUENCY REF – DIGITAL INPUT function is enabled, but the input to the receiver is missing or of a sample rate out of range. The OUT LOCK LED is always enabled.

7. VID LOCK LED: Enabled only if the OUTPUT FREQUENCY REF -NTSC VIDEO or OUTPUT FREQUENCY REF: PAL VIDEO (see OPERATION section) function is selected. Illuminates green if the video timing PLL is locked, red otherwise. The red condition typically indicates a missing or excessively noisy video signal, or a video signal of incorrect format.

8. AES/EBU and S/PDIF LED's: If the INPUT SOURCE ANALOG function is selected, indicates digital audio output format. If the INPUT SOURCE DIGITAL function is selected, indicates digital audio input and output format. If both the input and output formats are the same, one LED will illuminate. If format conversion between S/PDIF and AES/EBU is occurring, both LED's illuminate. Output format may then be determined from the LCD, as described in the OPERATION section. AES/EBU is used to indicate either AES/EBU or SMPTE, since the channel status definitions are the same for AES/EBU and SMPTE.

9. Bar-graph Display: Two 32 segment displays provide stereo input level indication. Each segment corresponds to 3 dB. Peak hold is utilized. The last segment of each channel is red, to represent an overload condition. Analog or digital input level is displayed corresponding to selection of the INPUT SOURCE ANALOG or INPUT SOURCE DIGITAL function, respectively. The bar graph display represents the signal prior to delay or pitch pressing. Thus, if the AD3100 is operating at an audio delay, the bar graph display will respond ahead of the output.

Operation

This section describes the operation of the AD3100.

Keypad summary

The 16 keys are arranged according to the following diagram:

DUMP	1	2	3
MODE/CLEAR	4	5	6
HELP	7	8	9
ENTER	±	0	.

Menu operation is organized by modes. Six modes are available--Pitch Shift, Remote Delay, Variable Delay, Fixed Delay, Time Compress/Expand, and Setup. The Setup mode contains a sub-menu of functions.

The MODE/CLEAR key scrolls through top menu mode selections. After a mode has been entered, pressing MODE/CLEAR resumes top menu scrolling.

The ENTER key is used for entering a displayed mode, enabling a displayed function, and for numerical value entry. Pressing the MODE/CLEAR key during numerical entry deletes entered numbers, and allows for the entry of a different value.

Pressing the HELP key displays applicable help information. For help messages too large for one screen, pressing the HELP key repeatedly causes display of the continuation of the message. Help is exited by pressing the MODE/CLEAR key.

The ± key is used to scroll through the Setup sub-menus. The ± key is also used to scroll through available function selections within each sub-menu. During a numeric entry, pressing the ± key at any time causes polarity reversal of the displayed value.

The DUMP key is used from a delay mode to produce an instantaneous zero delay, with subsequent loss of audio in memory. When the DUMP key is released, delay ramps back to the previously selected value.

Analog Input Level Adjustment

Two potentiometers on the front panel provide adjustment of the analog input level. Maximum CW rotation corresponds to the nominal full scale input levels as described in the SPECIFICATIONS and SETUP sections. CCW rotation attenuates the level applied to the analog-to-digital converter. A range of 0 to 20 dB attenuation is available.

Analog Output Level Adjustment

Two potentiometers on the front panel provide adjustment of the analog output level. Maximum CW rotation corresponds to the nominal full scale output levels as described in the

SPECIFICATIONS and SETUP sections. CCW rotation attenuates the analog output. A range of 0 to 20 dB attenuation is available.

Modes of Operation

When the AD3100 powers up, the display will show:

**PIXEL AD3100
DELAY CONTROLLER**

Pressing **MODE/CLEAR** enters the top menu.

1. Setup

The Setup mode provides for user specification of parameters related to input source, digital audio format, sample rate, frequency reference, delay change rate, time units and digital audio input error control.

To enter the setup mode, press **MODE/CLEAR** repeatedly until the display shows:

Setup Functions

Press **ENTER** to enter this mode. The next screen will be:

**Setup
Input Source**

Pressing **ENTER** again will cause the screen to show:

**Input Source
Analog ***

The "*" indicates the currently enabled selection (for purposes of illustration, it is here assumed that the default selections are enabled). Another indication that analog has been selected as the input source is that the **INPUT LED** is extinguished. Pressing \pm will cause the display to toggle between the above screen and the following:

**Input Source
Digital**

Pressing **ENTER** activates the displayed selection. Analog is the factory default.

In the Input Source Digital mode, the AD3100 receiver automatically locks to the incoming sample rate in the range from 25kHz to 48kHz, and determines and displays the format (AES/EBU or S/PDIF).

Pressing **MODE/CLEAR** returns the display to:

**Setup
Input Source**

Pressing the \pm key scrolls through the Setup sub-menu. The next sub-menu is:

Setup
Rate of Delay Change

Pressing ENTER will cause the screen to show:

Dly Rate Chnge xx.x%
Rate: 0.

The top line shows the rate at which the AD3100 performs delay changes. Factory default is 10.0%. The second line shows the new rate entry from the keypad. Pressing ENTER saves the new rate. A rate from 0.5% to 25.0% may be entered.

The next Setup sub-menu is:

Setup
Output Format

Pressing ENTER will cause the display to show:

Output Format
AES / EBU *

The "*" indicates the currently enabled selection. Pressing the \pm key will cause the display to toggle between the above screen and:

Output Format
SPDIF

Pressing ENTER activates the displayed selection. AES / EBU is the factory default. The AES / EBU selection is used to enable both, AES / EBU and SMPTE output formats.

The next Setup sub-menu is:

Setup
Output Sample Rate

If Input Source Analog has been selected, pressing ENTER will cause the screen to show:

Output Sample Rate
48 kHz *

The "*" indicates the currently enabled selection. Pressing \pm will sequence through the other available sample rates of 44.1, 44.056, and 32 kHz. Pressing ENTER selects a rate. If the screen shows,

Setup
Output Sample Rate

and Input Source Digital has been selected, pressing ENTER will cause the display to show:

Output Sample Rate
Auto

A selection of Auto causes the nominal output sample rate to be the same as the input sample rate. Pressing \pm will sequence through the other available choices of 48, 44.1, 44.056, and 32 kHz. 48 kHz is the factory default. The next Setup sub-menu is:

Setup
Output Frequency Ref

Pressing ENTER causes the screen to show:

Output Frequency Ref
NTSC Video

Pressing \pm will sequence through the other available choices of PAL Video, Input, and Xtal. Xtal corresponds to the internal free running reference, and is the factory default. Pressing ENTER activates a selection. An "*" indicates the currently enabled selection. If TIME VALUES – PAL (NTSC) FIELDS has been previously selected (see below), selecting NTSC (PAL) VIDEO for the frequency reference will cause the display to show:

Warning! Time units
and Reference differ

Pressing ENTER again will clear the warning message and enable selection.

The digital audio receiver of the AD3100 derives all necessary timing information from the incoming signal itself, and does not require an external reference. In order to maintain compatibility with the receiving unit connected to the AD3100 digital audio output, the AD3100 output sample rate may, however, need to be frequency locked to an external reference. This may be accomplished by selecting NTSC VIDEO or PAL VIDEO if the receiving unit uses a video reference signal. In this case, the video reference signal must be connected to the rear panel VIDEO 1 and VIDEO 2 loop-through connectors.

Appendix A details the frequency relationships between the video reference and AD3100 output sample rate. Alternatively, INPUT may be selected as the reference. In this case, the AD3100 output sample rate is frequency locked to the incoming sample rate from the source unit, and hence is frequency locked to the same reference used by the source. The lock ratios between output and input sample rates, when INPUT is selected as the reference, are also listed in Appendix A.

If XTAL is selected, the AD3100 digital audio output clock free runs, and will not be locked to any other unit which it may be connected to.

All selections in the Output Frequency Ref sub-menu are available for both analog and digital input modes.

The next Setup sub-menu is:

**Setup
Time Values**

This sub-menu is used to select the units of displayed and entered time quantities. Pressing ENTER will cause the display to show:

Time Values
Seconds *

Pressing \pm will sequence through the other available choices of NTSC FIELDS and PAL FIELDS. SECONDS is the factory default. If OUTPUT FREQUENCY REF- NTSC (PAL) VIDEO has been previously selected, selecting TIME VALUES – PAL (NTSC) FIELDS will cause the display to show:

**Warning! Time units
and Reference differ**

INPUT ERROR CONTROL DISABLED is the factory default. If the INPUT ERROR CONTROL DISABLED selection is activated, the AD3100 digital audio receiver may output random data if unlocked. Pressing \pm will cause the display to toggle between the above screen and:

Input Error Control
Repeat Last Sample

If the REPEAT LAST SAMPLE selection is activated, the digital audio receiver will output zeros if unlocked. The lost audio sample will be repeated if a confidence, lock, code, parity, or validity error (see FRONT PANEL DISPLAY AND INDICATORS section) is detected.

2. Pitch Shift

The AD3100 performs pitch modification, as controlled by keypad input. Pitch shift is available at any fixed zero or non-zero delay.

From the Setup Functions mode, pressing MODE/CLEAR will cause the display to show:

Pitch Shift
Delay: x.xxx Sec. (or xx.x Fields)

The second line displays the current delay. Pressing ENTER enters the mode:

Pitch xx.x %
Dly On (or Off), Pitch: 0.

The top line displays the current pitch shift. The second line indicates if the current delay is non-zero (Dly On) or zero (Dly Off). The second line also shows the new pitch entry from the keypad. Pressing ENTER saves the new pitch shift. Values between -25.0% and +25.0% may be entered.

Pitch shift is defined relative to the input. In many cases, it will be desired to use the pitch shift feature to correct pitch artifacts present on incoming material. In general, to correct pitch as

closely as possible, for incoming material with a pitch shift of X% relative to true, the AD3100 pitch shift, Y%, should be set as closely as possible to,

$$Y = \{ [100/(100 + X)] - 1 \} * 100\%.$$

For example, suppose the input source material is known to be 10% low in pitch. In this case, X equals -10. Therefore,

$$Y = \{ [100/(100 + -10)] - 1 \} * 100\% = +11.11111...%$$

A pitch shift of +11.1% should be entered. As a second example, if the incoming material is known to be 10% high in pitch, then X equals +10, and,

$$Y = \{ [100/(100 + 10)] - 1 \} * 100\% = -9.09090...%$$

A pitch shift of -9.1% should be entered.

When the entered pitch shift is returned to 0, delay returns to the original value within 13 seconds or less. If the MODE/CLEAR key is operated before the delay is restored, adjustment using the Fixed Delay or Variable Delay function may be required to return to the original delay.

3. Remote + Offset

The Remote + Offset mode derives the delay time from a steering input applied to the rear panel REMOTE DELAY or SERIAL IN connector. A delay which is the sum of the steering input and a user-specified offset results. The offset may be positive, negative, or zero. A default value of zero is assumed if no offset is entered. From the top menu display of:

Remote+Offset Delay
Delay: x.xxx Sec. (or xx.x Fields)

Pressing ENTER causes the display to show:

Delay x.xxx Sec. (or xx.x Fields)
Offset: 0.

The desired offset value, including sign, is entered on the second line.

4. Variable Delay

The variable delay mode allows the operator to manually increment or decrement the delay, using the keypad. From the top menu display of:

Variable Delay
Delay: x.xxx Sec. (or xx.x Fields)

Pressing ENTER causes the display to show:

Holding Delay
Delay: x.xxx Sec. (or xx.x Fields)

The “1” key is used to increase delay, and the “2” key is used to decrease delay. Pressing and holding the “1” key causes the display to show:

Increasing Delay
Delay: x.xxx Sec. (or xx.x Fields)

. Pressing and holding the “2” key causes the display to show:

Decreasing Delay
Delay: x.xxx Sec. (or xx.x Fields)

The displayed value is continuously updated. When both keys are released, the display returns to:

Holding Delay
Delay: x.xxx Sec. (or xx.x Fields)

In the variable delay mode, delay changes at a 0.5% rate, without pitch correction.

5. Fixed Delay

In the Fixed Delay mode, the user specifies the desired delay by entering it on the keypad. The top menu display for this mode is:

Fixed Delay: Pitch 0 (or + or -)
Delay: x.xxx Sec. (or xx.x Fields)

Pressing ENTER will cause the display to show:

Delay x.xxx Sec. (or xx.x Fields)
Pitch 0 (or + or -), Delay: 0.

The second line shows keypad numerical entry. After the desired delay is keyed in, pressing ENTER initiates delay change. Pitch shift is automatically applied when necessary during delay change to maintain minimum net throughput pitch modification. Additional pitch shift is not available during delay change. Thus, pitch shift will be deactivated, and the display will show:

Delay x.xxx Sec. (or xx.x Fields)
Pitch 0, Delay: x.xxx (or xx.x)

6. TIMEMAKER™ - Time Compress/Expand

The AD3100 may be used to alter the duration of audio material by changing the delay during playing of the material. The time compress/expand mode accomplishes this function. From the top menu display of:

Time Compress/Expand

Pressing ENTER causes the display to show:

Source Duration
Enter: 0. Sec

The second line shows the source duration entry from the keypad. Pressing ENTER saves the entry. Pressing MODE/CLEAR was before pressing ENTER clears the entry. Source duration of up to 3000 seconds may be accommodated. After the source duration is entered, the display shows:

Time Difference
Enter: 0. Sec

The second line shows the time difference entry from the keypad. A positive time difference indicates expansion, and negative time difference indicates compression. A time difference magnitude of up to 6 seconds may be accommodated. The entered time difference magnitude may be from +/- 0.2% to +/-10% of the source duration. Pressing ENTER saves the time difference. Pressing MODE/CLEAR once before pressing ENTER clears the entry.

If a positive time difference is entered, the AD3100 executes a dump to zero delay, and the display than shows:

**Press ENTER to start
expansion**

ENTER should be pressed simultaneously with the beginning of the Audio material. After ENTER is pressed, the display will show:

Expansion active
Percentage: xxx %

The percentage of completion increases from 0, and is continuously updated. When the completion percentage reaches 100, delay change ceases, and the display shows:

**Expansion
Complete**

If, after the source duration is entered, in negative time difference is then entered, the display will show:

Please wait
Preparing Delay

The AD3100 builds up the amount of delay required to implement the request of compression. When the delay is prepared, the display shows:

**Press ENTER to start
compression**

ENTER should be pressed at the same time the beginning of the audio material appears at the output of the AD3100. After ENTER is pressed, the display will show:

Compression active
Percentage: xxx %

The percentage display decreases from 100, and is continuously updated. When 0 is reached, delay change ceases, and the display shows:

Compression
Complete

Pressing MODE/CLEAR after expansion or compression is complete returns to the display:

Time Compress/Expand

Help Menu

From the top menu or from any mode, a help message can be displayed by pressing HELP. Messages too large to fit on one screen are continued by pressing HELP again. To exit help, press any other key.

1. From any top menu display, pressing HELP will display:

Press MODE to step
through the modes

Pressing HELP a second time will display:

Press ENTER to
select a mode

2. When the Setup Functions mode is selected, pressing HELP will display:

Press ± to step
through functions

Pressing HELP a second time will show:

Press ENTER to
select a function

When the Input Source function is selected, pressing HELP will show:

Press ± to step
through inputs

Pressing HELP a second time will display:

**Press ENTER to
select a input**

When the Rate of Delay Change function is selected, pressing HELP will show:

**Type rate of delay
change, press ENTER**

When the Output Format function is selected, pressing HELP will show:

**Press ± to toggle
output format**

Pressing HELP a second time will display:

**Press ENTER to
select output format**

When the Output Sample Rate function is selected, pressing HELP will show:

**Press ± to step
through sample rates**

Pressing HELP a second time will show:

**Press ENTER to
select a sample rate**

When the Output Frequency Ref function is selected, pressing HELP will display:

**Press ± to step
through references**

Pressing HELP a second time will show:

**Press ENTER to
select a reference**

When the Time Values function is selected, pressing HELP will show:

**Press ± to toggle
Seconds/Fields**

Pressing HELP a second time will show:

**Press ENTER to
select time mode**

If the display shows:

**Warning! Time units
and Reference differ**

Pressing HELP will show:

**ENTER will allow
difference**

Pressing HELP a second time will display:

**Set Time Values and
Output Frequency**

Pressing HELP a third time will display:

**Reference to the
same field units.**

When the Time Values function is selected, pressing HELP will display:

**Press ENTER to
disable or enable**

Pressing HELP a second time will display;

**Repeat Sample on
Error Option**

3. When the pitch shift mode is selected, pressing HELP will show:

**Type value, -25.0 to
+25.0 %. Press ENTER**

4. When the Remote+Offset Delay mode is selected, pressing HELP will show:

**Type offset delay
and press ENTER**

5. When the Variable Delay mode is selected, pressing HELP will show:

**Press 1 to increase
delay**

Pressing HELP a second time will display:

**Press 2 to decrease
delay**

6. When the Time Compress/Expand mode is selected, pressing HELP from the Source Duration display will show:

**Type source duration
and press enter**

Pressing HELP from the Time Difference display will show:

**-value = compression
+value = expansion**

Pressing HELP from the “Press ENTER to start expansion (compression)” display will show:

**Press ENTER to start
compress/expand**

7. When the fixed delay mode is selected, pressing HELP will show:

**Type Fixed Delay
and Press ENTER**

THEORY OF OPERATION

The diagram entitled “AD3100 BLOCK DIAGRAM” depicts audio and control signal flow. Reference designators and sheet numbers within dashed line ellipses refer to the schematic.

Please refer to schematic diagram “SCEM, AD3100”. Sheet 1 shows the interconnects for all subsequent sheets, which are numbered 2 through 13. Operation of sheets 2 through 13 is described below.

Regulator (Schematic AD3100, sheet 2)

DC power voltages +6V/+18.5V/-18.5V are applied to P2. Regulators U6, U5, U1, and U4 produce +5V, +12VD, +17V, and -17V, respectively. U184 produces -12V fan power. U2 and U3 monitor +5V, +17V, and -17V against a nominal tolerance of $\pm 10\%$. If an out-of-tolerance condition is detected, active low signal /PWR FAIL is asserted. /PWR FAIL will also be asserted if signal /695RST from sheet 7 is asserted.

Digital Audio RCV / XMIT (Schematic AD3100, sheet 3)

The AES/EBU balanced digital audio input signal from J8 pins 2 and 3 is applied to K8. K8, in conjunction with K7, bypasses J8 to J4 if signal DRDRV from sheet 9 is low, or if DC power is not present. Under normal operation, DRDRV is high, and the AES/EBU signal is applied to 1:1 transformer T1 pins 1 and 3. T1 pins 4 and 6 apply the balanced signal to E1 and E2, respectively. R20 provides a nominal 110 Ω termination.

The S/PDIF or SMPTE unbalanced digital audio input signal from J2 or J3 is applied to K6. K6, in conjunction with K5, bypasses J2/J3 to J5/J6 if DRDRV is low, or if DC power is not present. Under normal operation, the unbalanced signal is applied to E1. R30, in parallel with the input impedance of U7, provides a nominal 75 Ω termination.

Jumpers E1 and E2 select which digital audio input signal is applied to digital audio interface receiver U7. U7 pins 9 and 10 are RS-422 line receiver inputs.

U7 decodes the incoming serial data, and de-multiplexes stereo audio samples, channel status, parity, and validity bits. A PLL within U7 recovers timing information.

U7 accommodates any received sample rate from 25 to 48 kHz. The following signals are output from U7:

RMCK: Recovered clock at 256 times the incoming sample rate.

RSDATA: Serial stereo audio data in LSB last format. RSDATA is timed by RL//R and RCVSCK, derived from RMCK by circuits shown on sheet 5. RSDATA word length is 16, 18, or 20 bits, as determined by U7 register programming.

U7 control registers are programmed by the microcontroller (sheet 11), via address bus A[0..4] and data bus BAD[0..7]. Multiplexer U8 applies either A4 or clock signal 6.144MHZ to U7 pin 13. The 6.144MHz clock is used by U7 as the reference for measurement of input sample rate.

Normally, signal /A4 from sheet 11 is high. The microcontroller uses the A[0..4] and BAD[0..7] busses to read U7 status and buffer registers.

The status registers contain confidence, lock, code, parity, and validity bits, CRC error information, and a 3 bit received frequency code. U7 partitions received frequency into eight categories. Four of the categories are $48\text{kHz} \pm 400\text{ppM}$, $44.1\text{kHz} \pm 400\text{ppM}$, $44.056\text{kHz} \pm 400\text{ppM}$, and $32\text{kHz} \pm 400\text{ppM}$. If and only if one of these four categories is indicated, the microcontroller illuminates the corresponding front panel LED.

The buffer registers contain received channel status.

Digital audio interface transmitter U9 multiplexes, encodes, and transmits audio data, as well as validity, channel status, and parity bits. The following signals are input to U9:

TFSYNC: Frame synchronization signal in the form of a square wave at the sample rate.

TMCK: Master clock at 256 times the sample rate for 48, 44.1, or 44.056 kHz, or 384 times the sample rate for 32 kHz.

TXSCK: Audio data bit clock at 64 times the sample rate.

TSDATA: Audio data. Normally, audio data 1890DO from sample rate converter U63 (sheet 6) is selected by the presence of a jumper at JP9 pins 2 and 3 (indicated as "N" on the PC board silkscreen). For purposes of bit error rate testing (please see Appendix B for more information), RSDATA may be connected directly to TSDATA by moving the jumper at JP9 to pins 1 and 2 (indicated as "BER" on the PC board silkscreen).

U9 control and buffer registers are loaded via busses A[0..4] and BAD[0..7]. The buffer registers are loaded with channel status data for transmission.

Signals /8401CS, /8411CS, and /CRW control read and write operations from and to U7 and U9.

RS-422 driver U11 buffers the output from U9 pin 20, and applies differential signal output to 1:1 transformer T3. Output from T3 is routed to AES/EBU output connector J4 through bypass relay K7. R31, in series with the internal output resistance of U11, provides a nominal $110\ \Omega$ source resistance.

Resistive dividers R23/R25 or R22/R24, in conjunction with a $75\ \Omega$ impedance load at J5 or J6, attenuate the output from U11 pin 20 to 5 V p-p or 1 V p-p, respectively. Output level is selected by the positions of jumpers at E3 and E4. Output from E4 pin 2 is routed to J5/J6 through 1:1 transformer T2 and bypass relay K5.

Connector J7 carries signals to the front panel bar graph display. U185C and 20 bit audio data signal 157SDATA with 96-kHz square wave /96 kHz, to produce the 16 bit audio data signal needed by the bar graph display. U13 delays and buffers audio bit clock SCLKOUT, for routing to the bar graph display.

Data and Timing (Schematic AD3100 sheet 4)

A-to-D conversion, audio digital signal processing (DSP), and D-to-A conversion in the AD3100, all take place at a fixed 48 kHz sample rate. This rate is derived from the 12.288 MHz clock U106, found on sheet 9.

Signal 12.288MHz, from sheet 9, is divided by two by U35A, to produce signal 6.144MHz, and divided by two again, by U35B, to produce 3.072 MHz clocks at U35B pins 9 and 10. The output from U35B pin 10 clocks binary counters U36 and U37. U36 and U37, J/K flip-flops U42A and U42B, and associated gates, form a 64-state finite state machine. This state machine generates bit and word clocks used by the A-to-D, D-to-A, and DSP circuits. Clocks SPROC SCLK, 5390SCLK, 5842BCKI, and 1890SCLK are all audio data bit clocks occurring at 3.072 MHz. U36 and U37 count from 0 to 63, with U36 pin 14 as the LSB, and U37 pin 13 the MSB. Signals 5390L//R, CL0, and 1890L//R, are word clocks at 48 kHz. 5390L//R, CL0, and 1890L//R are derived directly from U37 pin 13, and thus transition at counts 0 and 32. Signal VU/L//R is the inverted version of 1890L//R. Signal 5842LRCl, a word clock at 48 kHz, transitions at counts 20 and 52. U40F pin 12 is low during counts 0 through 19 and 31 through 51, and high otherwise. This signal is applied to the INHIBIT inputs (pin 6) of parallel-in-serial-out shift registers U20, U21, U22, U23, and U44. U41A pin 3 is low during count 31, and high otherwise. U41A pin 3 is connected to the SHIFT/LOAD inputs (pin 15) of U20, U21, U22, U23, and U44.

Shift registers U20, U21, U22, U23, and U44 convert parallel audio data output from DSP U81 (sheet 7) into serial audio data suitable for input to interpolation filter U117 (sheet 10). 20 bits each left and right audio data, from U81 parallel data bus DATA[0..23] are latched into octal D-type flip flops U14 through U19. U14, U15, and U16 are clocked by signal /LOWE. U17, U18, and U19 are clocked by signal /ROWE. Parallel output from U14 through U19 are applied to the shift register parallel data inputs. The shift registers latch this data at the transition from count 31 to count 32 of U36/U37, as set up by the above described signals from U40F pin 12 and U41A pin 3. Right channel audio data is serially output at 3.072 MHz from U20 pin 13 during counts 0 through 19 of U36/U37. Left channel data is output from U20 pin 13 during counts 32 through 51 of U36/U37.

Switch S1 has two positions--"normal", denoted by "N" on the PC board silkscreen, and "not delayed", denoted by "ND" on the silkscreen. S1 controls multiplexer U24. When S1 is in the "N" position, U24 routes the data from U20 to E5 pin 1. When S1 is in the "ND" position, U24 routes signal 157SDATA to E5 pin 1. 157SDATA represents input data from either the A-to-D converter or U7. Therefore, the "ND" position of S1 bypasses the DSP (U81). Jumper E5 selects either normal operation (pins 1 and 2 connected), denoted by "N" on the silkscreen, or loop mode (pins 2 and 3 connected), denoted by "LOOP". In the loop mode, signal TESTDATA, a delayed version of R48DATA, which in turn is data from U7 after conversion to 48 kHz, is passed to the D-to-A converter, even if INPUT SOURCE – ANALOG function is selected by front panel keypad entry. This allows a loop-back test of the digital audio transmitter and receiver. Detailed information on the loop mode is contained in Appendix B.

JP10 is always open.

The U24 pin 4 output is also passed, as signal 1890DIN, to sample rate converter U63 (sheet 6), for conversion to the digital audio transmit rate.

Octal D-type flip flops U25, U26, and U27 latch a 19 bit number, representing current audio delay in units of 1/48000 Sec., as output by U81's parallel data bus DATA[0..23]. U25, U26, and

U27 are clocked by signal /CDWE. The microcontroller, U153, reads the outputs of U25, U26, and U27 via bus BAD[0..7], under control of signals /CDHI, /CDMID, and /CDLO.

U153 writes audio target delay to U32, U33, and U34. The target delay is read by U81, via DATA[0..23], under control of signal /TARGETRE. Parameters related to the control of the DSP algorithms are written to U28 through U30 by U153, and are read by U81.

Input Sample Rate Conversion (Schematic AD3100 sheet 5)

U46, U45, U47, U50A, and associated gates form a finite state machine which provides timing for U7 and the input portion of sample rate converter U51. Signal RMCK from U7 clocks 8-bit binary counter U46 at 256 times the digital audio received sample rate. U46 counts from 0 to 255. U46 pin 7 outputs left/right clock signal RL//R. RL//R transitions at counts 0 and 128, and is applied to both U7 pin 11 and U51 pin 5. The signal from U46 pin 1, at 64 times the received sample rate, is inverted by U49B to form bit clock RCVSCK. RCVSCK is applied to both U7 pin 12 and U51 pin 4.

The position of the MSB of RSDATA relative to RL//R depends on whether U7 is programmed for 16, 18, or 20 bit output. RSDATA MSB is identified by the rising edge of the word clock signal applied to U51 pin 5. This signal is generated by U45, U46, U47, U48, U49A, and U50A. U47 is loaded by U153 with 3Fh, 37h, or 2Fh, for word lengths 16, 18, or 20 bits, respectively. Corresponding counts from U46 are decoded modulo 128 by identity comparator U45. The output from U45 is applied to the J input of U50A, through U49A. U50A pin 6 outputs a rising edge at the beginning of counts 64/192, 56/184, or 48/176, for word lengths of 16, 18, or 20 bits, respectively. U48 causes the resetting of U50A pin 6 at the beginning of counts 0/128.

U51 performs conversion of the RSDATA sample rate to a rate of 48 kHz. The resultant is audio data signal R48DATA. R48DATA is output in MSB first format, and is timed by signals 1890SCLK and 1890L//R. R48DATA word length is 24 bits, of which up to 20 are used by subsequent circuits. U51's processor clock is supplied by signal 18MHZ from sheet 6.

Multiplexer U52, under control of signal /DIGITAL from sheet 1, selects either signal TESTDATA (a buffered version of R48DATA), or signal 5390_SDATA_IN (from A-to-D converter U104). U52 output 157SDATA is applied to the bar graph display, as previously explained, as well as to DSP U81.

Signal 2XTMCK, from sheet 6, is divided by two by U187B to generate signal TMCK, for application to U9 of sheet 3. U62 divides 2XTMCK by two or three, under control of signal 3//2 from sheet 11. A division ratio of three is used for a transmitted sample rate of 32 kHz. A division ratio of 2 is used for all other transmitted rates. The output from U62A pin 6 clocks 8-bit counter U55 at 256 times the transmit sample rate. U54, U55, U53, U49E, and U56A generate a word clock for identifying the MSB of the transmitted serial audio, in a like manner to that described above for the receive word clock as generated by U45, U46, U48, U49A, and U50A. Transmit and receive word lengths are always identical, since U47 connects to both U45 and U54. The transmit word clk, TXWCLK, is applied to U63 pin 25. TL//R, output by U56B pin 10, is a 50% duty cycle signal at the transmit sample rate, which transitions at the same time as the positive-going edge of TXWCLK.

Multiplexer U58, under control of signal /FRAMELOCK from sheet 11, selects either U55 pin 7 or U46 pin 7 to produce signal TFSYNC. TFSYNC, a 50% duty cycle waveform at the transmit

sample rate, is utilized by U9. In normal operation, /FRAMELOCK is high, and TFSYNC transitions coincidentally with the negative-going edge of TXWCLK. /FRAMELOCK will be low only during the BER test mode, where data is passed directly from U7 to U9, and direct frame synchronization between U7 and U9 must be maintained.

U61 and U59 provide regulated +12V and -12V for circuits on sheet 6.

Output Sample Rate Conversion (Schematic AD3100 sheet 6)

U63 converts the 48 kHz sample rate of signal 1890DIN to the transmit sample rate. 1890DIN is timed by signals 1890L//R and 1890SCLK. The output serial data from U63 pin 23 is timed by signals TXSCK, TL//R, and TXWCLK. TXWCLK is high for the particular word length of 16, 18, or 20 bits, and is ANDed with the the 24 bit word from U63 pin 23. Thus, resultant serial data 1890DO is truncated to the proper length prior to being applied to U9.

Signal 2XTMCK is generated by a phase locked loop frequency synthesizer formed by U64, U65, U66, U67, U68, and associated components. Multiplexer U64, under control of signals REFMUX0 and REFMUX1 from sheet 11, selects 12.288MHZ, RMCK, or 18MHZ, corresponding to a reference selection of Xtal, Input, or NTSC/PAL Video, respectively. The output of U64 is applied to synthesizer U65 reference input "FR", pin 1. U68A and associated components form a voltage controlled oscillator (VCO). The output from U68A is buffered by U68B, and applied to the input of divide-by-20/21 dual modulus prescaler U66. The output from U66 is applied to U65's "FIN", pin 8. U65 contains programmable reference and frequency dividers, dual-modulus control logic, a three-state phase-frequency detector, and a lock detector. Divide ratios are programmed serially via signals SERDATA, SERCLK, and 58_ENAB from sheet 11. The reference input at U65 pin 1 is divided by U65 to a comparison frequency between 11.278 kHz and 28.8 kHz, depending on reference and output frequency selection, and applied to the phase-frequency detector. The divide ratio programmed to be applied to the frequency input at pin 8 is selected to produce the proper output frequency at U68A pin 2. The divided frequency input is also applied to the phase-frequency detector. The phase-frequency error voltage is output from U65 pin 5. This error voltage is differentially integrated relative to 2.5 VDC by U67 and associated components. The output voltage from U67 is applied to varactors D21 through D24, to control the VCO frequency. When the loop is locked, a voltage of 2.5 VDC is present at U65 pin 5.

When the loop is locked, the lock detector output from U65 pin 7 consists of a high logic level voltage, with very narrow negative-going spikes of repetition rate equal to the phase-frequency detector comparison frequency. This voltage is filtered by R39 and C105, and produces negative-true lock indication signal /MAINLOCK at U60E pin 10. If the loop is not locked, the negative-going pulses from U65 pin 7 have a much higher duty factor. These pulses are stretched by D20, and result in a high level at /MAINLOCK.

18MHZ is phase locked to the externally applied video horizontal sync if NTSC or PAL video is selected as the reference. Base-band video applied to loop through connectors J9 and J10 is buffered by U71 and associated components. U71 is configured as a high input impedance differential amplifier, operating on the video input signal and return. This configuration minimizes loop through loading, and provides common-mode rejection. Sync stripper U73 outputs horizontal sync at pin 15. Multiplexer U10 applies the U73 output to U69 pin 1, under control of signals VIDMUX0 and VIDMUX1 from sheet 11. PLL frequency synthesizer U69 is similar to U65, except that it does not have dual-modulus control capability. U69's divide ratios

are programmed serially by SERDATA, SERCLK, and 57_ENAB from sheet 11. The horizontal rate, H, input to "OSCIN", U69 pin 1, is divided by three, prior to application to U69's phase-frequency detector. Signal 18MHZ, input to "FIN", U69 pin 8, is divided by 3432 for NTSC or 3456 for PAL. Differential phase-frequency detector outputs, pins 15 and 16, are applied to a loop amplifier comprised of U70 and associated components. The loop amplifier is connected as a differential integrator. 18 MHz voltage controlled crystal oscillator (VCXO) U72 is tuned by the voltage output from U70 pin 1. Signal 18MHZ is output by U72 pin 8. Thus, the frequency of this signal is $1144 * H$ or $1152 * H$, for NTSC or PAL, respectively. U60F and associated components operate on the lock detector output from U69 pin 7, in a like manner to that described above for U65 etc. U60F outputs negative-true lock indication signal /VIDLOCK.

Digital Signal Processing (Schematic AD3100 sheet 7)

DSP U81 executes the audio pitch shift and delay algorithms. Audio serial data signal 157SDATA is input to U81 pin 92. Data timing is provided by signals 5390L//R, applied to U81 pins 91 and 95, and SCLKOUT, applied to U81 pin 88. Parallel data bus DATA[0..23], address bus ADRS[0..15], write signal /WRSPR, read signal /RDSPR, and chip select /CSSPR allow U81 to communicate with the audio delay memory of sheets 12 and 13, and control and data registers of sheet 4.

Upon power-up, reset generator U76 resets U81. When U81 comes out of reset, an internal bootstrap routine loads the DSP program from EPROM U74 into internal RAM. When program loading is complete, execution begins. Execution is triggered by 48 kHz signal CL0, applied to U81 pin 67.

Access port connector J12 allows communication with internal registers of U81. DAC U79 provides an analog representation of internal U81 registers under access port or U74 program control. Switched-capacitor filter U80 may be used to filter the output from U79. U80 has a cutoff frequency of 15.625 kHz, or .01 times the U80 clocking signal 1.5625MHZ. J12, U79, and U80 are provided for factory test use, and are not used during normal operation. Headers J11, J13, and J14 are used only as test points. Locations J11-J14, U79 and U80 may not to have components installed.

S2 provided manual reset capability for factory test use. S2 is not used during normal operation.

D25, driven by the U81 "/BUSY", pin 103, glows in response to parallel bus activity.

Signal /695RST to sheet 2 from U76 pin 15 is asserted if +5VD drops below a nominal 4.65 V.

Serial Remote Bus (Schematic AD3100 sheet 8)

A remote delay pulse applied to J17 is converted to logic levels by U82C. The high period of the remote delay pulse is counted in units of 102.4 microseconds by a 16 bit counter formed by U87, U88, U89, and U90. The delay count is applied to octal D-type flip flops U91 and U92. The delay count may then be read via BAD[0..7] by U153 on sheet 11.

Alternatively, remote delay may be input serially via J15. Data is applied to J15 pin 1, and clock to J15 pin 3. The serial data is clocked into shift-and-store bus registers U94 and U93. U94 and U93 may also be read via BAD[0..7].

J16 provides remote dump capability. When continuity is provided between the tip and shield of J16, Q2 conducts between signal lines P1.0 and P1.4, connecting to sheet 11.

Analog to Digital Conversion (Schematic AD3100 sheet 9)

The left channel analog audio input from J18 is applied to K1. K1, in conjunction with K3 of sheet 10, bypasses J18 to J23 if signal /PWR_FAIL from sheet 2 is low, or if power is not present. In normal operation, the left audio is applied to a differential amplifier comprised of U98, U116, U107 and associated components. Switch S4, along with R163, R164, R202, and potentiometer connected to J19, selects the input full scale level. The potentiometer connected to J19 also provides front panel gain trim. The single ended signal output from J19 is buffered and converted back to a differential signal by U109 and U108. The outputs from U109 and U108 are applied to the left input of A-to-D converter U104.

In a like manner, the right channel input from J21 is processed by U100, U99, U114, S6, U101, and U113, and applied to the U104 right input. Gain trim is provided by the potentiometer connected to J20. K2 bypasses J21 to J25 (sheet 10) via K4 (sheet 10) if power is not present or /PWR_FAIL is asserted.

Crystal oscillator U106 generates 12.288 MHz master clock, used by U104. Word and bit timing for U104 is provided by signals 5390L//R and 5390SCLK, from sheet 4. Serial data output from U104 is buffered by U183A to form a signal 5390_SDATA_IN.

A DC servo loop comprised of U115, U111, U112, and U104 is used to trek out any DC offset which may be present in the input amplifiers. DC offset present on the incoming signal will also be tracked out if the magnitude of the offset is not too large. One shots U115A and U115B are triggered on alternate edges of 5390L//R. The active low output pulses of U115A/B are approximately 160 ns in duration, and are applied to three-state bus driver U111 gate inputs /1G and /2G respectively. Audio data 5390_SDATA_IN is applied to U111 input pins 10 and 12. Corresponding U111 output pins 9 and 11 are applied to inverting integrators U112A/B and associated components. The gating action of U115 causes the sign bit of the audio left and right channels to be applied to U112A and B, respectively. The applicable U11 outputs are high impedance the rest of the time. The average sign bit level is integrated relative to 2.5VDC, as set by R209/R210 and R204/R206. The integrator outputs are fed back to the U104 analog inputs by corresponding to the minimum DC offset. The bandwidth of this feedback loop is very low, so as not to adversely impact the audio response.

Digital to Analog Conversion (Schematic AD3100 sheet 10)

Serial audio data signal 5842DIN, from sheet 4, is applied to 8X over-sampling interpolation filter U117. 8X over-sampled left and right outputs from U117 are applied to 20 bit DAC's U118 and U120, respectively. The current outputs from U118 and U120 pin 6 are converted to voltage by U136B and U138B, respectively.

The voltage output from U136B is filtered by a generalized impedance converter low-pass reconstruction filter formed by U137 and associated components. The filter output is buffered by U136A, and output to J22. J22 connects to a front-panel potentiometer, which provides output gain trim. The audio signal from the potentiometer wiper is buffered and amplified by U126. U126 operates at a gain level of 0, 4, or 8 dB, as set by S7. These three gain levels correspond to full scale output levels of +20, +24, and +28 dBu, respectively. The output from U126 he is

applied to an inverting amplifier comprised of U121, U135, and associated components, and to a non-inverting amplifier comprised of U122, U134, and associated components. The outputs from U134 and U135 produce a balanced signal at the left channel output connector J23.

In a like manner, right channel DAC voltage output from U138B is processed by reconstruction filter / buffer U139 and U138A, the potentiometer connected to J24, selectable gain amplifier U127, and balanced output amplifiers U123/U133 and U124/U132, to produce output at the right channel output connector J25.

Controller (Schematic AD3100 sheet 11)

The controller operates the front panel keyboard, LCD, and indicator LED's. It also operates the rear panel RS-232 interface; responds to rear panel TTL pulse, serial remote delay, or dump inputs; programs the digital audio receiver and transmitter IC's U7 and U9 respectively; reads and processes incoming and digital audio channel status bits; generates digital audio channel status for transmission; programs synthesizer IC's U65 and U69; controls the generation of certain timing signals; processes alarm status bits; selects analog and digital input source; provides pitch shift and delay control inputs to the DSP; and reads and displays current delay.

EPROM U141 stores the program for microprocessor U153. Address/Data bus multiplexing is performed by U140. Parallel communication with data and control registers associated with other sections of the AD3100 is carried out via buffered address/data bus BAD[0..7].

Connector JP5 connects to the front panel keyboard. Connector JP6 connects to the front panel LCD. LCD drive signals are obtained from U153 bus AD[0..7], and from multiplexed address bus A[0..7] via PLD U143. Front panel LED indicators for digital audio sample rates, format selection, and alarms are driven from the display driver U188. Data is shifted serially into U188 from U153. Communication with RS-232 remote connector P1 is accomplished via transceiver U146.

Serial remote bus data from sheet 8 is read on BAD[0..7] under control of strobe signals /REMOTE1 and REMOTE2 emanating from PLD U144.

U153 accesses registers of digital audio receiver and transmitter IC's U7, and U9, via A[0..4] and BAD[0..7], along with chip select signals /8401CS and /8411CS, and are read and/write control line /CRW. U153 loads the control registers of U7 and U9, reads the status registers of U7 and U9, reads the incoming channel status buffer of U7, and loads the outgoing channel status buffer of U9.

Synthesizers U65 and U69 are loaded serially by signals SERCLK and SERDATA. And data is strobed into U65 or U69 and by 58_ENAB or 57_ENAB, respectively. Lock alarms /MAINLOCK and /VIDLOCK are strobed into U147 to be read by U153.

Capability to place DSP U81 in reset is provided by signal /SPROCRESET output from U143 pin 10. PLD's U144 and U145 generate the other control signals, as described above for schematic sheets 4, 5, and 6.

U152 sources the 50 MHz master clock for U81. U149, U151, and U150 divide 50 MHz down to the 9.766 kHz clock required by U87 through U90 of sheet 8. A 1.5625 MHz clock is output from U151 for use by U80 of sheet 7.

Memory 1 and Memory 2 (Schematic AD3100 sheets 12 and 13)

External RAM for U81 is organized as 786432 words by 20 bits. The 16 most significant bits are arranged as six pairs of 131072 x 8 SRAM's, represented by U164 through U175. The 4 least significant bits are arranged as three 262144 x 4 SRAM's, denoted as U180, U181 and U182. Data is written to and read from memory by U81, via 24 bit data bus DATA[0..23] and 16 bit address bus ADRS[0..15]. Since a 20 bit address is required to access 786432 locations, for bits are effectively added to ADRS by multiplexing DATA 16 through DATA 19 via octal D flip-flop U155.

Locations 04000h-0FFFFh, 14000h-1FFFFh, 24000h-2FFFFh, and so forth up through B4000h-BFFFFh are used for delayed stereo audio sample data. Locations 00000h-00FFFh are reserved for U81 internal addresses. Locations 01000h-0100Fh are used for memory-mapped register enable addresses. Locations 01010h-03FFFh and 2110h-23FFFh are used to store data related to pitch correction. The remaining locations are not used.

PLD U154 places signal /CE1 in the active (high) state for addresses in the range 01000h-0100Fh, deselecting all SRAM's. Addresses in this range, along with a right, read, and chip select signals /WRSPR, /RDSPR, and /CSSPR, are decoded by PLD U157 to produce individual register enable signals. Read enable signals/TARGETRE, /SLEW1RE, SLEW2RE cause the corresponding registers on sheet 4 to place outputs the bus. Data read when /SLEW1RE or /SLEW2RE is asserted occupies the 16 most significant bits. Whenever /SLEW1RE or SLEW2RE is asserted, /LSEWRE is also asserted, causing tri-state octal buffer U1777 to place zeroes on the bus for the lowest 8 bits. Write enable signals /CDWE, /ROWE and /LOWE clock data into corresponding registers on sheet 4.

Signal /HCE, decoded by U154, gates DATA[16..19] into U155, synchronous to /WRSPR, to form the upper 4 bits of memory address.

/CE1 is asserted for all active addresses above 0100Fh, allowing the SRAM to be selected. If either ADRS14 or ADRS15 is one, analogous to addresses X4000h-XFFFh, SRAM's U57D, U158, U159A U159B, U160 U161, U162, U178 and U179. Signals CE20 through CE25 each select a unique pair of 131072 x 8 SRAM's. The lower half of U180, U181 or U182 is selected at the same time that CE21, CE23, or CE25, respectively is asserted. Additionally, U 155 pin 2 is gated to all SRAM A16 inputs in the form of signal ADRS16.

If ADRS14, ADRS15, GP0 and /CE1 are all zero, locations 01010h-03FFFh become active. In this case, U165, U166 and the lower half of U180 are selected, and ADRS16 is forced to zero.

If ADRS14, ADRS15, and /CE1 are zero and GP0 is one, locations 21010h-23FFFh become active. In this case, U164, U166 and the upper half of U180 are selected, and ADRS16 is forced to zero.

Whenever /CE1 and U81 read strobe /RDSPR are both asserted, tri-state octal buffer U176 places zeroes on the bus in the four least significant data bit positions.

PC BOARD ADJUSTMENTS

1. LCD Display Viewing Angle: While observing the LCD display, adjust R269 until the desired result is obtained.
2. Adjustment of video reference high frequency common-mode rejection: Apply a sine wave signal of amplitude approximately 1 V pk-pk and frequency approximately 1 MHz simultaneously to both the center and outer contacts of J9. Monitor TP10 on an oscilloscope, using a 10X probe. Connect the probe ground lead to TP25. Adjust C115 for minimum signal.
3. Adjustment of main PLL tuning range: Allow unit to warm up for at least 20 minutes before making this adjustment. Select "Xtal" Output Frequency Ref. Select 48 kHz Output Sample Rate. Monitor TP59 on a frequency counter, using a 10X oscilloscope probe. Connect the probe ground lead to TP25. Verify that the front panel OUT LOCK LED is illuminated green, and that the counter reads $12,288,000 \pm 300$ Hz. Measure the voltage at TP44 relative to TP25. Adjust L8 so that TP44 measures $+6.5 \pm .5$ VDC relative to TP25.
4. Adjustment of DC CMRR: With no connection made to analog input connectors, install jumpers at JP3/JP4. Monitor TP34/TP33 with an oscilloscope probe. Connect the probe ground to TP27. Apply a DC voltage, variable from -5 VDC to +5 VDC, between TP31/TP29 and TP27. Adjust R160/R177 for minimum change at TP34/TP33 when the voltage between TP31/TP29 and TP27 is varied between -5 VDC and +5 VDC. When this adjustment is completed, remove jumpers from JP3/JP4.
5. Adjustment of AC CMRR: With no connection made to analog input connectors, install jumpers at JP3/JP4. Monitor TP34/TP33 with an oscilloscope probe. Connect the probe ground to TP27. Apply a 10 kHz, 10 V pk-pk sine wave signal between TP31/TP29 and TP27. Adjust R159/R176 for minimum AC component at TP34/TP33. When this adjustment is completed, remove jumpers from JP3/JP4.

APPENDIX A

Output sample rates as related to selected source.

A1. Output Frequency Reference: Input Audio

Output sample rate relationship to input sample rate

Input Rate (kHz)	Selected Output Rate (kHz)			
	32	44.056	44.1	48
32	1/1	1575/144	441/320	3/2
44.056	1144/1575	1/1	1001/1000	572/525
44.1	320/441	1000/1001	1/1	160/147
48	2/3	525/572	147/160	1/1

A2. Output Frequency Reference: NTSC Video

Output sample rate as function of NTSC horizontal (H) rate

Output Rate Selected (kHz)	Output Rate, Locked to Video (kHz)
32	2288H/1125
44.056	14H/5
44.1	7007H/2500
48	1144H/375

A3. Output Frequency Reference: PAL Video

Output sample rate as function of PAL horizontal (H) rate

Output Rate Selected (kHz)	Output Rate, Locked to Video (kHz)
32	256H/125
44.056	2016H/715
44.1	1764H/625
48	384H/125

APPENDIX B

Test Modes

The AD3100 may be configured for two test modes, “Loop”, and “Bit Error Rate Test”.

The loop mode is useful for verifying the basic functionality of the digital audio transmitter or receiver against the digital audio receiver or transmitter, respectively. To utilize this mode, E5 must be placed in the LOOP position, and JP9 must remain in the “N” position. With this configuration received digital audio, after conversion to 48 kHz sample rate, is passed directly to the digital-to-analog converters. A cable must be connected from one of the digital audio outputs to the appropriate digital audio input. Additionally, the analog input source must be selected, and the output frequency reference must be XTAL, NTSC VIDEO, or PAL VIDEO. An analog signal applied to R INPUT and L INPUT will then be converted to digital, subjected to the pitch shift or delay operation as may be selected in the normal manner, output as digital, routed by external cable to the digital audio input, converted to analog, and appear at connectors R OUTPUT and L OUTPUT. Any available digital audio sample rate may be used.

In the BER mode, received digital audio sample data is passed directly to the transmitter, without any intervening rate conversion(s). If a suitable test instrument is connected between the AD3100 digital audio input and output connectors, bit error performance of the transmission channel formed by the AD3100 receiver, AD3100 transmitter, interconnecting cables, and the test instrument, may be measured. The Audio Precision model System One Dual Domain, running the BITTEST real-time program, is an example of a suitable test instrument. JP9 must be placed in the BER position. Additionally, the AD3100 must be placed in the BER mode using the RS-232 remote interface. The output and input sample rates must be the same. Only audio sample bits are tested. All other sub-frame bits, such as validity, user data, channel status, and parity, are not tested by the BER mode. A constant-value waveform should not be used for bit error testing if the INPUT ERROR CONTROL-REPEAT LAST SAMPLE function has been selected.

APPENDIX C

Additional jumpers, connectors and switches

The following jumpers, connectors, and switches appear on the PC board. Modification of the following jumper or switch positions from the factory setting, or use of any of the following connectors, is not required for normal operation.

1. E5: Jumper position selects normal or loop mode, as described in Appendix B. "Normal" is the factory default position.
2. JP1: Selects U81 master or slave mode. Jumper not installed selects master mode, jumper installed selects slave mode. **For normal operation jumper must not be installed.**
3. JP2: Jumper position selects upper or lower half of address space of DSP program PROM U74. **Must be installed toward front panel.**
4. JP3, JP4, JP10: Not used in normal operation. **Must not have any jumpers installed.**
5. JP8: Jumper position selects A/D converter (U104) power-up offset calibration mode. When installed to the right as seen from the front panel side of the unit, calibration inputs are obtained from analog ground; this is the recommended, as well as the factory default, setting. When installed to the left as seen from the front panel side, calibration inputs are obtained from the U104 analog input pins.
6. JP9: Jumper position selects normal or bit error rate test mode as described in Appendix B. "Normal" is the factory default position.
7. J11, J12, J13, J14: Not used in normal operation. **Must not have any connectors or jumpers installed.**
8. S1: Selects "normal" or "non-delayed" operation. The "N" position, which is the factory default, selects normal operation. Selection of the "ND" position causes the delay and pitch shift processing to be bypassed.
9. S2: Momentary pushbutton for manual reset of U81. It does not apply in normal operation.
10. S9: Momentary pushbutton for manual reset of U153. It does not apply in normal operation.